WHAT IS CLAIMED IS:

1. An analog-to-digital converter for converting an input voltage into a plurality of digital signals, through serial-parallel conversion, each of said plurality of digital signals being comprised of N bits data where N is an integer of not less than two, the converter comprising:

a partial voltage generation circuit which generates a plurality of partial voltages for said N bits by means of dividing a reference voltage;

high-bits side comparators for comparing said input voltage with each partial voltage, said each partial voltage being in a part of said plurality of partial voltages, which becomes data of high bits whose bit number is more than half of the N bits;

a high-bits side encoding circuit which encodes comparison results from said high-order comparators and outputs said encoded comparison results as high-bit data having said bit number of said high bits ;

selection circuits for selecting a part of said partial voltages, which becomes data of low bits with a bit number being defined as half of the plurality of said N bits, in accordance with said comparison results of said high-bits side comparators;

low-bits side comparators for comparing each partial voltage of said partial voltages selected by said selection circuits with said input voltage;

a low-bits side encoding circuit which encodes comparison

outputs from said low-bits side comparators and outputs said encoded comparison results as low-bit data having said bit number of said low bits; and

a logic circuit which outputs N bits data based on a matching being made between the high-bit data and the low-bit data, wherein

when said matching stands between the high-bit data and the low-bit data, said N bits data is output in accordance with predetermined conditions, while when said matching does not stands in-between, said high-bit data is modified according to said low-bit data,

and said N bits data is output in accordance with predetermined conditions .

2. The analog-to-digital converter according to claim 1, wherein said N bits data is defined by 2n bits, where said high-bit data is defined by n+1 bits, and said low-bit data is defined by "n" bits.

3. The analog-to-digital converter according to claim 1 or 2, further comprising:

a sample-and-hold circuit which samples and holds an input signal from the outside every sampling cycle to generate said input voltage;

high-bits side latch circuits which latch comparison outputs from said high-bits side comparators and input said latched comparison outputs to said high-bits side encoding

circuit; and

low-bits side latch circuits which latch comparison outputs from said low-bits side comparators and input said latched comparison outputs to said low-bits side encoding circuit,

wherein said high-bits side latch circuits and said low-bits side latch circuits perform latching operations at different timing within the same cycle of said sampling cycle.